REMARKS

This paper responds to the Office Action dated on April 4, 2005.

Claims 1, 3, 5, 6, 8, 11, 15-18 and 20-23 are amended, no claims are canceled, and claims 25-27 are added; as a result, claims 1-27 are now pending in this application.

§103 Rejection of the Claims

Claims 1, 2, 4, 5, and 7-24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Shibata et al. (U. S. Patent No. 5,754,838) in view of IBM (16 Mb Double Data Rate Synchronous Graphics RAM). Applicant respectfully traverses the rejection, and submits that the claims amendments contained herein place the claims in condition for allowance.

The cited reference of Shibata discloses a synchronous DRAM (SDRAM) that has an internal clock different from the external clock signal (col. 3, lines 3 to 7) using a PLL circuit included in the clock input buffer 1. Shibata is a synchronous DRAM and discloses halting the operation of the PLL and using the external clock as the internal clock using a test mode for "developing and designing devices" (see column 15, lines 1-2). The cited reference does not teach a SDRAM operating without synchronizing the internal clock to the external clock except as a test, and not as an operational mode.

The cited reference of IBM, which is cited by applicant and incorporated by reference on page 3 of applicant's specification, is seen as teaching one, and only one, of the two commonly known modes of operation of a dual data rate SGRAM as discussed in applicant's specification at least at page 7, second paragraph where the first mode is a non-DLL mode and the second mode is the IBM mode of using the DLL at all operations. Applicant submits that a power down mode is not operating a memory device, nor is a test mode or a refresh mode properly considered an operational mode.

In summary, the cited reference of Shibata teaches a SDRAM that is always in DLL or PLL mode when operational, plus the ability to adjust the DLL to operate stably in various external clock speed ranges. The cited reference of IBM teaches a SGRAM that is always in DLL mode when operational. Neither discloses normal operation in non PLL mode.

With a view to improving the clarity of Applicant's device, which among other features, can have two operational modes, as distinct from the non operational test modes of the cited

references, the independent claims have been amended herein to clarify that the two modes of the present invention are two operational modes that allow operation of the memory with different industry standard memory operational modes. As noted in the specification at least at pages 2 and 7, the two main industry standard operational modes are the JEDEC standard for synchronous operation using a DLL or a PLL circuit and exemplified by the cited IBM RAM above, and the non synchronous mode exemplified by the Intel and Samsung device KM432D5131 DDR SGRAM revision 0.6 April 1998, incorporated by reference in the present application. Thus Applicant respectfully submits that the present amended claims make it clear that the cited references are distinctly different since they teach a single operational mode, and a non operational mode such as test mode, or a refresh mode.

Specifically, the suggested combination of references neither describe nor suggest at least the combination of features of "*...a logic circuitry coupled to the memory array configurable to operate the single memory device in a first operational mode having delayed lock loop (DLL) capability and in a second operational mode having non-DLL capability ...*", as recited in independent claims 1 and 5, as amended herein. As the Examiner noted on page 4 of the outstanding Office Action, both prior art references discuss not using the DLL during either test mode or internal memory refresh modes, and that the claims of the present subject matter should be interpreted broadly without importing limitations from the specification. Applicant respectfully submits that the present claim amendments have made the present subject matter clearly distinct over any combination of the cited references, whether taken alone or in any combination with other well known art, by clarifying that the two modes are operational modes.

Specifically, the suggested combination of references neither describe nor suggest at least the combination of features of "*...to operate in a first operational mode and a second operational mode, the first operational mode and the second operational mode each relating to a different alignment of output data as to a read line of the memory for different industry standard operational modes for memory devices ...*", as recited in claims 8, 11, 13, 15 and 20, as amended herein. The reasons are similar to those given above, and for providing industry standard operational modes. Thus the independent claims are believed to be in patentable condition.

The dependent claims are seen as being in patentable condition at least as depending upon independent claims shown above to be patentable over the suggested combination of cited

art. In view of the above noted claims amendments and discussion contained herein, Applicant respectfully requests that this rejection be reconsidered and withdrawn.

Allowable Subject Matter

Claims 3 and 6 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant has amended the application to rewrite claim 3 and 6 in independent form, and requests that claims 3 and 6 be passed to allowance.

Applicant further requests that dependent claims 25-27 be entered and allowed as these claims depend from claims 3 and 6.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

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Date 6 June '05

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 6 day of June, 2005.

Tina Kohel
Name

Signature